BLF6G15L-40RN; BLF6G15LS-40RN Power LDMOS transistor

AMPLEON

Rev. 3 — 1 September 2015

Product data sheet

Product profile

1.1 General description

40 W LDMOS power transistor for base station applications at frequencies from 1450 MHz to 1550 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25$ °C in a class-AB production test circuit.

Test signal	f	V _{DS}	P _{L(AV)}	Gp	η _D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	1476 to 1511	28	2.5	22.5	13.5	-45 <mark>[1]</mark>

^[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 8.4 dB at probability of 0.01 % on CCDF carrier; carrier spacing 5 MHz.

1.2 Features and benefits

- Typical 2-carrier W-CDMA performance at frequencies of 1476 MHz and 1511 MHz, a supply voltage of 28 V and an I_{Dq} of 375 mA:
 - ◆ Average output power = 2.5 W
 - ◆ Power gain = 22.5 dB
 - ◆ Efficiency = 13.5 %
 - ◆ ACPR = -45 dBc
- Easy power control
- Integrated ESD protection
- Enhanced ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1450 MHz to 1550 MHz)
- Internally matched for ease of use
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC.

1.3 Applications

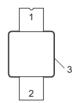
RF power amplifiers for W-CDMA base stations and multi carrier applications in the 1450 MHz to 1550 MHz frequency range

2. Pinning information

Table 2. Pinning

	•			
Pin	Description		Simplified outline	Graphic symbol
BLF6G15	L-40RN (SOT1135A)			
1	drain			
2	gate		1	
3	source	[1]		2 — 3 sym112
BLF6G15	LS-40RN (SOT1135B)			
1	drain			







3. Ordering information

Table 3. Ordering information

Type number	Packag	Package		
	Name	Description	Version	
BLF6G15L-40RN	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT1135A	
BLF6G15LS-40RN	-	earless flanged ceramic package; 2 leads	SOT1135B	

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+11	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
$R_{\text{th(j-case)}}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 2.5 W (CW)	1.30	K/W

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^[1] Connected to flange.

6. Characteristics

Table 6. Characteristics

 $T_i = 25$ °C per section; unless otherwise specified

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 0.59 \text{ mA}$	65	-	-	V
V _{GS(th)}	gate-source threshold voltage	V_{DS} = 10 V; I_{D} = 59 mA	1.4	1.8	2.4	V
I _{DSS}	drain leakage current	$V_{GS} = 0 \text{ V}; V_{DS} = 28 \text{ V}$	-	-	1.4	μА
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	9.4	-	Α
I _{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
9 _{fs}	forward transconductance	V_{DS} = 10 V; I_{D} = 58.9 mA	-	0.5	-	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 2.06 \text{ A}$	-	0.32	-	Ω

7. Application information

Table 7. 2-carrier W-CDMA RF performance

Class-AB production test circuit; PAR 8.4 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz; 3GPP test model 1; 64 DPCH; f_1 = 1476 MHz; f_2 = 1511 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 375 mA; T_{case} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$P_{L(AV)}$	average output power		-	2.5	-	W
Gp	power gain	$P_{L(AV)} = 2.5 W$	19.8	22.5	-	dB
RLin	input return loss	$P_{L(AV)} = 2.5 W$	-	-16	-11	dB
η_{D}	drain efficiency	$P_{L(AV)} = 2.5 \text{ W}$	11.5	13.5	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 2.5 W$	-	-45	-40	dBc

7.1 Ruggedness in Class-AB operations

The BLF6G15L-40RN and the BLF6G15LS-40RN are capable of withstanding a load mismatch corresponding to VSWR 10 : 1 through all phases under following conditions: $V_{DS} = 28 \text{ V}$; $I_{Dq} = 375 \text{ mA}$; $P_L = 40 \text{ W}$; f = 1476 MHz (CW).

8. Test information

8.1 Impedance information

Table 8. Typical impedance

Measured load-pull data. Typical values per section. $I_{Dq} = 330$ mA; main transistor $V_{DS} = 28$ V Z_S and Z_L defined in Figure 1.

f	Z _S	Z _L
(MHz)	(Ω)	(Ω)
1450	4.4 – j5.9	5.5 – j4.6
1480	4.4 – j4.1	5.0 – j5.0
1510	6.4 – j4.7	5.0 – j5.0

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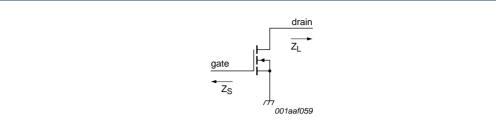
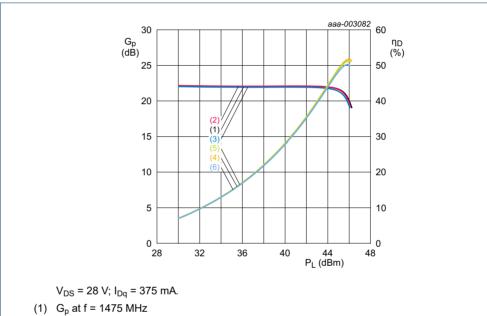


Fig 1. Definition of transistor impedance

8.2 One-tone graphs

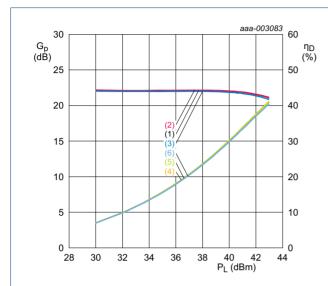


- (1) Opati : 110 iii i=
- (2) G_p at f = 1493 MHz
- (3) G_p at f = 1511 MHz
- (4) η_D at f = 1475 MHz
- (5) η_D at f = 1493 MHz
- (6) η_D at f = 1511 MHz

Fig 2. Power gain and drain efficiency as function of load power; typical values

8.3 2-Carrier W-CDMA graphs

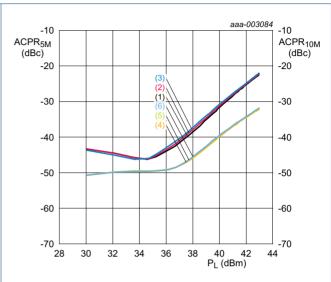
3GPP, test model 1; 64 DPCH, PAR = 8.4 dB at 0.01 % probability, 5 MHz carrier spacing.



 $T_{amb} = 25 \, ^{\circ}C.$

- (1) G_p at f = 1475 MHz
- (2) G_p at f = 1493 MHz
- (3) G_p at f = 1511 MHz
- (4) η_D at f = 1475 MHz
- (5) η_D at f = 1493 MHz
- (6) η_D at f = 1511 MHz

Fig 3. Power gain and drain efficiency as function of load power; typical values

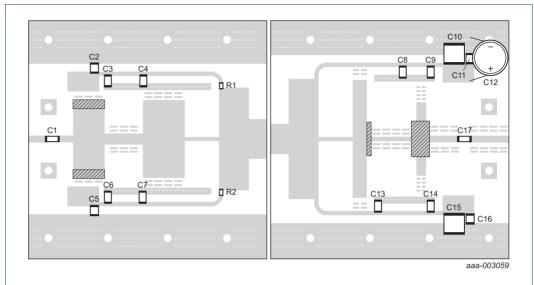


 $T_{amb} = 25 \, ^{\circ}C.$

- (1) ACPR_{5M} at f = 1475 MHz
- (2) ACPR_{5M} at f = 1493 MHz
- (3) ACPR_{5M} at f = 1511 MHz
- (4) ACPR_{10M} at f = 1475 MHz
- (5) ACPR_{10M} at f = 1493 MHz
- (6) ACPR_{10M} at f = 1511 MHz

Fig 4. Adjacent channel power ratio (5 MHz and 10 MHz) as a function of load power; typical values

8.4 Test circuit



Striplines are on a double copper-clad Rogers R04350 Printed-Circuit Board (PCB) with ϵ_r = 3.5, thickness = 0.762 mm and thickness copper plating = 35 μ m.

See Table 9 for list of components.

Fig 5. Component layout for test circuit

Table 9. List of components For test circuit, see Figure 5.

Component	Description	Value	Remarks
C1, C17	multilayer ceramic chip capacitor	24 pF	<u>[1]</u>
C3, C6	multilayer ceramic chip capacitor	68 pF	[2]
C4, C7, C8	multilayer ceramic chip capacitor	150 pF	[2]
C9, C14	multilayer ceramic chip capacitor	47 pF	[2]
C13	multilayer ceramic chip capacitor	15 pF	[2]
C2, C5, C11, C16	multilayer ceramic chip capacitor	10 μF	[3]
C10, C15	multilayer ceramic chip capacitor	0.1 μF	[3]
C12	electrolytic capacitor	2200 μF, 50 V	
R1, R2	chip resistor	15 Ω	

^[1] American technical ceramics type 800B or capacitor of same quality.

^[2] American technical ceramics type 100B or capacitor of same quality.

^[3] TDK or capacitor of same quality.

9. Package outline

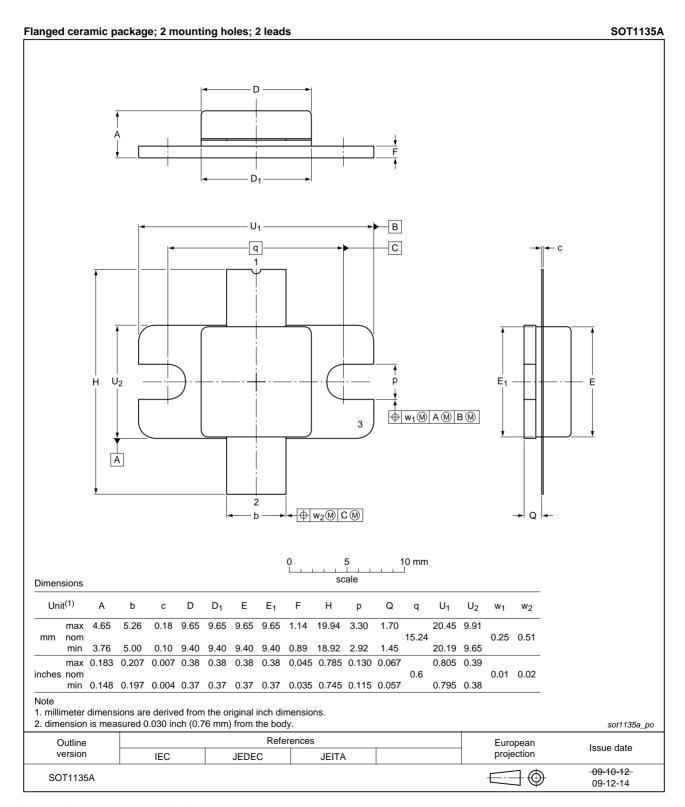


Fig 6. Package outline SOT1135A

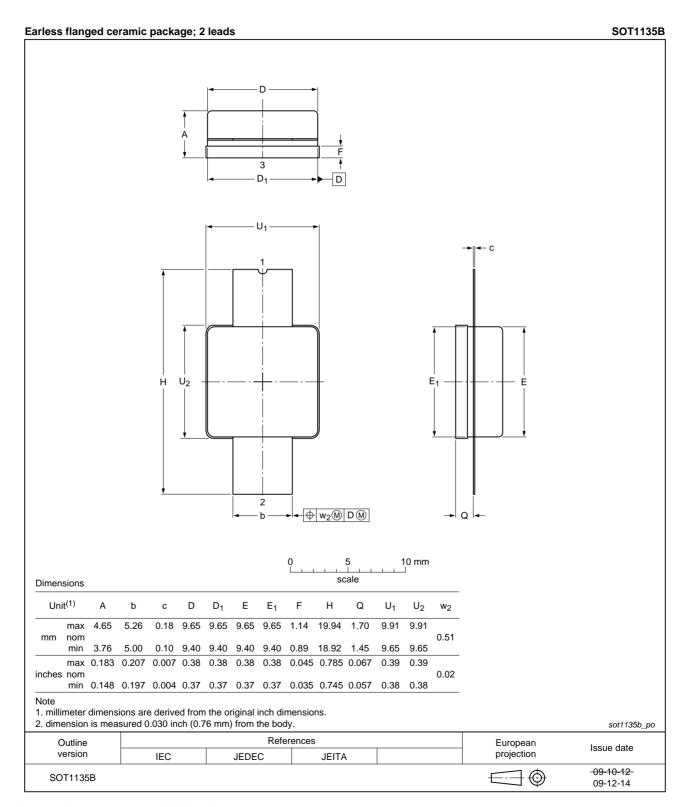


Fig 7. Package outline SOT1135B

10. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

11. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical Channel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PAR	Peak-to-Average Ratio
RF	Radio Frequency
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
BLF6G15L-40RN_6G15LS-40RN#3	20150901	Product data sheet	-	BLF6G15L-40RN_6G15L S-40RN v.2	
Modifications:	 The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. Legal texts have been adapted to the new company name where appropriate. 				
BLF6G15L-40RN_6G15LS-40RN v.2	20120514	Product data sheet	-	BLF6G15L-40RN_6G15L S-40RN v.1	
BLF6G15L-40RN_6G15LS-40RN v.1	20111027	Objective data sheet	-	-	

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13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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Power LDMOS transistor

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Power LDMOS transistor

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